REMARKS

Claim 22 is amended to correct a typographical error and not for purposes of patentability. Claims 1-30 remain for consideration, and all claims are thought to be allowable over the cited art.

The Office Action fails to establish that claims 1-30 are unpatentable under 35 USC §103(a) over "Balakrishnan" (US patent no. 6,135,647 to Balakrishnan et al.). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by Balakrishnan, fails to provide a proper motivation for modifying the teachings of Balakrishnan, and fails to show that the modification could be made with a reasonable likelihood of success.

Claim 1 sets forth a method for re-targeting a design. The Office Action fails to show that Balakrishnan teaches or suggests the limitations of receiving a first low-level design representation targeting a first integrated circuit; transforming said first low-level design representation into a synthesizable, editable, and simulatable high-level design representation; and processing said high-level design representation to generate a second low-level design representation targeting a second integrated circuit.

For example, the Office Action errs in citing Balakrishnan's FIGs. 3, 4, 5, and col. 4, l. 61 – col. 5, l. 43 as teaching the limitations of receiving a first low-level design representation targeting a first integrated circuit. None of the cited portions make any apparent reference to a low-level design. And the cited portions appear to teach the opposite, processing of high-level design.

Furthermore, the Office Action fails to show a suggestion of transforming said first low-level design representation into a synthesizable, editable, and simulatable high-level design representation. Balakrishnan teaches a SynRTL library having C++ classes representative of RTL constructions of Verilog or VHDL (col. 4, l. 61 – col. 5, l. 12). Thus, there is no apparent transformation of a low-level design representation into the claimed high-level design implementation.

The alleged motivation for modifying Balakrishnan to generate a second low-level design representation targeting a second integrated circuit is improper. The

alleged motivation states "that it would have been obvious ... to find that Balakrishnan RTL translator for HDL level system would imply the claimed limitation of a second low-level design representing targeting a second integrated circuit because the RTL code translates HDL code for a target device independent of technology as disclosed in Balakrishnan above." This alleged motivation is based on a false premise, unsupported by evidence, and therefore, improper.

The false premise of the alleged motivation is that Balakrishnan's HDL independent system is suggestive of different targeted devices. Those skilled in the art will recognize that Balakrishnan's system teaches a system for representing a design that is independent of a hardware description language, not independent of an integrated circuit (Abstract). Thus, the premise of the motivation is false, and the motivation is improper.

The alleged motivation also unsupported by any evidence. For example, no evidence is provided to support a motivation of modifying Balakrishnan to generate the low-level design representation for a second integrated circuit from the low-level design for a first integrated circuit.

Claims 2-5 depend from claim 1, and the Office Action fails to establish that these claims are unpatentable for at least the reasons set forth above.

Claims 6, 7, and 8 include limitations of and related to specific hardware description languages to which the low-level design representation is translated. As explained above in regards to claim 1, Balakrishnan is not shown to suggest any transformation from a low-level design representation to a high-level design representation. Thus, even though Balakrishnan may mention VHDL and Verilog as examples of HDLs, there is no correspondence to these HDLs to the claimed languages to which a low-level design representation is transformed.

Claim 10 includes further limitations of the transforming of the low-level design representation to the high-level design representation. As explained above in regards to claim 1, Balakrishnan is not shown to suggest any such transformation. Therefore, the further limitations of claim 10 are not shown to be suggested by Balakrishnan.

Claim 11 depends from claim 10 and includes further limitations of identifying equations in said first low-level design representation that give rise to synthesizable

and simulatable objects, the objects including flip-flops. The Office Action cites no specific portion of Balakrishnan as suggesting these limitations, nor does Balakrishnan's object oriented library appear to suggest any identification of equations that give rise to flip-flops. Thus, claim 11 is not shown to be suggested by Balakrishnan.

Claims 12-21 include a variety of additional limitations for which the Office Action makes only a general assertion that Balakrishnan suggests the limitations. The limitations of these claims, which include the context of the base and intervening claims, are not shown to be suggested by any specific teaching of Balakrishnan. Furthermore, Balakrishnan is not understood to suggest any of the specific limitations. Therefore, claims 12-21 are not shown to be unpatentable over Balakrishnan.

Claims 22-30 in many instances include limitations similar to those of claims 1-21, and the Office Action cites the same portions of Balakrishnan in rejecting claims 22-30 as are cited in rejecting claims 1-21. Therefore, the Office Action fails to show that claims 22-30 unpatentable over Balakrishnan for at least the reasons set forth above. Furthermore, the claims include limitations not addressed by the Office Action, such as in claim 22 with the first low-level design representation being targeted to a first type of integrated circuit and the second low-level design representation being targeted to a second, differnet type of integrated circuit. No teaching of Balakrishnan is cited as suggesting the claimed transformation from a low-level design representation for one type of device to a high-level design and then to a low-level design for a second, different type of device as claimed. Therefore, claims 22-30 are not shown to be unpatentable over Balakrishnan.

The rejection of claims 1-30 over Balakrishnan should be withdrawn because the Office Action fails to show all the limitations are suggested by Balakrishnan, fails to provide a proper motivation for modifying Balakrishnan, and fails to show that the modification could be made with a reasonable likelihood of success.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 14, 2005.

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